517,464

(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property Organization
International Bureau

(43) International Publication Date
18 December 2003 (18.12.2003)

PCT

(10) International Publication Number
WO 03/105341 A1

(51) International Patent Classification[7]: H03H 11/46, H03F 3/60, G01R 31/02

(21) International Application Number: PCT/SE02/01092

(22) International Filing Date: 6 June 2002 (06.06.2002)

(25) Filing Language: English

(26) Publication Language: English

(71) Applicant *(for all designated States except US)*: **TELEFONAKTIEBOLAGET LM ERICSSON (PUBL)** [SE/SE]; S-126 25 Stockholm (SE).

(72) Inventor; and

(75) Inventor/Applicant *(for US only)*: **BLADH, Mats** [SE/SE]; Önnemovägen 116, S-146 53 Tullinge (SE).

(74) Agent: **ERICSSON AB**; Patent Unit Service and Backbone Networks, S-126 25 Stockholm (SE).

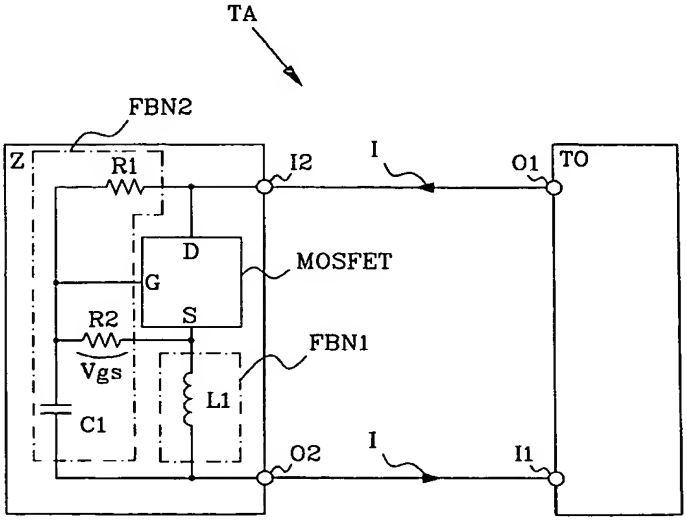
(81) Designated States *(national)*: AE, AG, AL, AM, AT, AU, AZ, BA, BB, BG, BR, BY, BZ, CA, CH, CN, CO, CR, CU, CZ, DE, DK, DM, DZ, EC, EE, ES, FI, GB, GD, GE, GH, GM, HR, HU, ID, IL, IN, IS, JP, KE, KG, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MA, MD, MG, MK, MN, MW, MX, MZ, NO, NZ, OM, PH, PL, PT, RO, RU, SD, SE, SG, SI, SK, SL, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VN, YU, ZA, ZM, ZW.

(84) Designated States *(regional)*: ARIPO patent (GH, GM, KE, LS, MW, MZ, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian patent (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European patent (AT, BE, CH, CY, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE, TR), OAPI patent (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

Published:
— *with international search report*

For two-letter codes and other abbreviations, refer to the "Guidance Notes on Codes and Abbreviations" appearing at the beginning of each regular issue of the PCT Gazette.

(54) Title: ACTIVE LOAD ARRANGEMENT



(57) Abstract: The present invention relates to an active load arrangement Z used to provide proper output load to an object TO under test. The arrangement Z comprises a voltage controlled transistor MOSFET having a source S, a gate G and a drain D. The drain D is associated with the gate G and connected to an arrangement input I2 associated with an output O1 of the object under test. The source S is connected to an arrangement output O2 associated with an input I1 of the object under test. A feedback arrangement is connected to the source S and the gate G. The feedback arrangement changes phase and amplitude of the gate-to-source voltage by varying frequency in order to obtain low impedance at low impedance at low frequencies and high impedance at high frequencies.

WO 03/105341 A1